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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,645	03/06/2002	Donald C. Soltis JR.	10016693-1	8480

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EXAMINER	
VITAL, PIERRE M	

ART UNIT	PAPER NUMBER
2188	4

DATE MAILED: 03/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,645	SOLTIS, DONALD C.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed February 18, 2004 in response to PTO Office Action mailed November 18, 2003. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. Claims 1-11 have been presented for examination in this application. In response to the last Office Action, claims 1, 5 and 11 have been amended. No claims have been canceled or added. As a result, claims 1-11 are now pending in this application.

3. The objection to the specification has been withdrawn due to the amendment filed February 18, 2004.

4. The previous rejection of claims 1-11 in the Office Action mailed November 18, 2003 (Paper No. 2) has been withdrawn due to the amendment filed February 18, 2004. New grounds of rejection follow herewith.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otterness et al (US6,460,122) and Akashi et al (US6,438,658) and further in view of Liao et al. (US6,681,296).

As per claim 1, Otterness discloses a processor integrated circuit capable of executing more than one instruction stream comprising:

a first processor, coupled to fetch instructions and access data through a first cache controller [*processing resources are multiple-processors and multiple-controllers combination*; col. 6, lines 45-52; *controllers move data to and from cache*; col. 5, lines 19-22]; a second processor, coupled to fetch instructions and access data through a second cache controller [*processing resources are multiple-processors and multiple-controllers combination*; col. 6, lines 45-52; *controllers move data to and from cache*; col. 5, lines 19-22]; a plurality of cache memory blocks, each containing data memory [*the number of blocks is set equal to the size of the host write request*; col. 11, lines 1-15]; a high-speed interconnect coupling the plurality of cache memory blocks to the first and second cache controllers such that at least one allocable cache memory block is capable of being used by the first and second cache controllers [*communications fibre loop interconnects cache controller A and cache controller B and the caches in controllers A and B*; Fig. 11; *controllers communicates with each other when moving data to*

and from and invalidating in any cache; data in any cache other than level 0 is considered shared data; col. 5, lines 19-24].

However, Otterness does not specifically teach a resource allocation controller coupled to determine an accessing cache memory controller selected from the group consisting of the first and second cache memory controllers, wherein the accessing cache memory controller has access to the allocable cache memory block as recited in the claim.

Akashi discloses a resource allocation controller coupled to determine an accessing cache memory controller selected from the group consisting of the first and second cache memory controllers, wherein the accessing cache memory controller has access to the allocable cache memory block [*node control circuit 150 whether the line exists in external cache and is controlled by cache control circuit 140 contained in each node; if the line exists in external cache, control circuit 150 sends it to processor 105a-1*; col. 11, lines 17-26].

It would have been obvious to one of ordinary skill in the art, having the teachings of Otterness and Akashi before him at the time the invention was made, to modify the system of Otterness to include a resource allocation controller coupled to determine an accessing cache memory controller selected from the group consisting of the first and second cache memory controllers, wherein the accessing cache memory controller has access to the allocable cache memory block because it would have ensured the consistency of caches in all the processors by checking whether the most recent data exists on each of the caches in all the remaining processors [col. 2, lines 8-11] as taught by Akashi.

However, Otterness and Akashi does not specifically teach that the cache memory blocks are usable by the cache controllers to store data and instructions fetched from a random access memory as recited in the claim.

Liao discloses the use of cache memory blocks usable by the cache controllers to store data and instructions fetched from a random access memory for increasing the speed of application by minimizing the need to access the relatively slow main memory (col. 2, lines 11-20). It is noted that main memory is made of DRAM as is well in the art. Since the technology for implementing the use of cache memory blocks usable by the cache controllers to store data and instructions fetched from a random access memory was well known, and since the use of cache memory blocks usable by the cache controllers to store data and instructions fetched from a random access memory for increasing the speed of application by minimizing the need to access the relatively slow main memory, an artisan would have been motivated to implement the use of cache memory blocks usable by the cache controllers to store data and instructions fetched from a random access memory in the system of Otterness and Akashi. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use cache memory blocks usable by the cache controllers to store data and instructions fetched from a random access memory because this feature was well known to benefit by increasing the speed of application by minimizing the need to access the relatively slow main memory.

As per claim 2, Otterness further discloses a plurality of first level cache systems [*multilevel cache and multiprocessor system*; col. 3, lines 61-66], wherein the first processor fetches instructions and accesses data from the first cache controller through a first level cache system, and wherein the second processor fetches instructions and accesses data from the second cache controller through a second first level cache system [*if data is present in higher level cache, initiating and completing data movement form a higher level cache to the level 0 cache by sending a cache data move message to the cache controller which has the data*; col. 25, lines 18-64].

As per claim 3, Otterness discloses the claimed invention as detailed above in the previous paragraphs. However Otterness does not specifically teach the cache memory blocks further comprise cache tag memory as recited in the claims.

Akashi discloses cache memory blocks comprising cache tag memory [*cache memory comprises a cache tag portion*; col. 3, lines 25-27].

It would have been obvious to one of ordinary skill in the art, having the teachings of Otterness and Akashi before him at the time the invention was made, to modify the system of Otterness to include cache memory blocks comprising cache tag memory because it would have provided a higher system throughput and reduced system latency by reading the cache tag portion of the memory to determine whether or not a block stored in the cache memory is available [col. 3, lines 47-50] as taught by Akashi.

7. Claims 4-6, 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otterness et al (US6,460,122) and Akashi et al (US6,438,658) and Liao et al. (US6,681,296) and further in view of Dean et al (US6,604,174).

As per claim 4, the combination of Otterness and Akashi and Liao discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Otterness and Akashi and Liao does not specifically teach each cache controller is provided with cache hit rate monitoring apparatus as recited in the claim.

Dean discloses each cache controller is provided with cache hit rate monitoring apparatus [*for each process, an expected or desired cache hit ratio is used to calculate miss percentage*; col. 9, lines 32-35].

It would have been obvious to one of ordinary skill in the art, having the teachings of Otterness and Akashi and Liao and Dean before him at the time the invention was made, to modify the system of Otterness and Akashi and Liao to include each cache controller is provided with cache hit rate monitoring apparatus because it would have provided a dynamic cache allocation based on performance by using a relational cache miss percentage to reallocate the ways [col. 3, lines 52-56] as taught by Dean.

As per claim 5, Otterness discloses a method of dynamically allocating cache on a multiple-processor integrated circuit, where the multiple processor integrated circuit is used in a partitionable multiple-processor system and comprises:

a plurality of processors each coupled to receive instructions from a first level cache associated therewith [*multiple processors execute RAID primitives or instructions; data readily available to the processor (i.e., instruction) will be referred to as level 0 cache*; col. 4, lines 17-45], a plurality of allocable upper level cache memory blocks [*cache lines were allocated*; col. 11, lines 9-19], interconnect apparatus for transmitting cache misses at each first level cache to upper level cache memory blocks assigned thereto [*communications fibre loop interconnects cache controller A and cache controller B and the caches in controllers A and B*; Fig. 11; *requested data not present in level 0 cache, initiate and complete data movement from higher level cache to level 0 cache*; col. 25, lines 18-52].

However, Otterness does not specifically teach an allocation apparatus for assigning upper level cache memory blocks to processors as recited in the claim.

Akashi discloses an allocation apparatus for assigning upper level cache memory blocks to processors [*node control circuit 150 whether the line exists in external cache and is controlled by cache control circuit 140 contained in each node; if the line exists in external cache, control circuit 150 sends it to processor 105a-1*; col. 11, lines 17-26] to ensure the consistency of caches in all the processors by checking whether the most recent data exists on each of the caches in all the remaining processors (col. 2, lines 8-11). Since the technology for implementing an allocation apparatus for assigning upper level cache memory blocks to processors was well known and since an allocation apparatus for assigning upper level cache memory blocks to processors ensure the consistency of caches in all the processors by checking whether the most recent data exists on each of the caches in all the remaining processors, an artisan would have been motivated to implement an

allocation apparatus for assigning upper level cache memory blocks to processors in the system of Otterness. Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Otterness and Akashi before him at the time the invention was made, to modify the system of Otterness to include an allocation apparatus for assigning upper level cache memory blocks to processors as taught by Akashi because it would have ensured the consistency of caches in all the processors by checking whether the most recent data exists on each of the caches in all the remaining processors [col. 2, lines 8-11] as taught by Akashi

However, Otterness and Akashi does not specifically teach that the cache memory blocks are usable by the cache controllers to store data and instructions fetched from a random access memory as recited in the claim.

Liao discloses the use of cache memory blocks usable by the cache controllers to store data and instructions fetched from a random access memory for increasing the speed of application by minimizing the need to access the relatively slow main memory (col. 2, lines 11-20). It is noted that main memory is made of DRAM as is well in the art. Since the technology for implementing the use of cache memory blocks usable by the cache controllers to store data and instructions fetched from a random access memory was well known, and since the use of cache memory blocks usable by the cache controllers to store data and instructions fetched from a random access memory for increasing the speed of application by minimizing the need to access the relatively slow main memory, an artisan would have been motivated to implement the use of cache

memory blocks usable by the cache controllers to store data and instructions fetched from a random access memory in the system of Otterness and Akashi. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use cache memory blocks usable by the cache controllers to store data and instructions fetched from a random access memory because this feature was well known to benefit by increasing the speed of application by minimizing the need to access the relatively slow main memory.

However, the combination of Otterness and Akashi and Liao does not specifically teach monitoring past cache performance associated with processors and partitions; determining desired processor to partition and upper level cache block allocations to processors; repartitioning the system, the step of repartitioning the system including allocation of upper level cache blocks to processors of at least one of the multiple processor integrated circuits as recited in the claim.

Dean discloses monitoring past cache performance associated with processors and partitions [*cache miss percentage is compared to the total misses of all the processes to determine if cache should be reallocated*; col. 4, lines 48-65]; determining desired processor to partition and upper level cache block allocations to processors [*for processes needing a large amount of cache space, tag allocation controller 161 can increase the number of ways allocated to these processes*; col. 5, lines 2-11]; repartitioning the system, the step of repartitioning the system including allocation of upper level cache blocks to processors of at least one of

the multiple processor integrated circuits [*allocation controller 161 reallocates ways of the cache to processes having the highest number of misses*; col. 6, lines 58-64].

It would have been obvious to one of ordinary skill in the art, having the teachings of Otterness and Akashi and Liao and Dean before him at the time the invention was made, to modify the system of Otterness and Akashi and Liao to include monitoring past cache performance associated with processors and partitions; determining desired processor to partition and upper level cache block allocations to processors; repartitioning the system, the step of repartitioning the system including allocation of upper level cache blocks to processors of at least one of the multiple processor integrated circuits as taught by Dean because it would have provided a dynamic cache allocation based on performance by using a relational cache miss percentage to reallocate the ways [col. 3, lines 52-56] as taught by Dean.

As per claim 6, Otterness discloses the upper level cache blocks are second level cache blocks [*level 1 or secondary cache of Otterness corresponds to upper level cache of the claimed invention, they are not local to the processor*; col. 4, lines 42-50].

As per claim 8, Otterness discloses the multiple processor integrated circuit further comprises a plurality of non-allocable cache memory blocks [*dirty cache lines must be flushed and are non-allocable*; col. 9, lines 53-60].

As per claim 10, the combination of Otterness and Akashi and Liao and Dean discloses the claimed invention as detailed above in the previous paragraphs. Otterness further discloses cache comprising cache data memory [*data cache in processor complex A, B, C*; Fig. 9-11].

However, Otterness does not specifically teach each upper level allocable cache block further comprises tag memory and cache data memory as recited in the claim.

Akashi discloses each upper level allocable cache block further comprises tag memory and cache data memory [*cache tag memory 125 and cache data memory 145*; Fig. 1].

It would have been obvious to one of ordinary skill in the art, having the teachings of Otterness and Akashi and Liao and Dean before him at the time the invention was made, to modify the system of Otterness and Liao and Dean to include cache memory blocks comprising cache tag memory because it would have provided a higher system throughput and reduced system latency by reading the cache tag portion of the memory to determine whether or not a block stored in the cache memory is available [col. 3, lines 47-50] as taught by Akashi.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Otterness et al (US6,460,122) and Akashi et al (US6,438,658) and Liao et al. (US6,681,296) and Dean et al (US6,604,174) and further in view of Itskin et al (US5,809,537).

As per claim 9, the combination of Otterness and Akashi and Liao and Dean discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Otterness and Akashi and Liao and Dean does not specifically teach an interconnect apparatus comprising a plurality of upper level cache controllers, and where each upper level cache controller is capable of controlling operation of the allocable cache memory blocks as a writeback cache as recited in the claim.

Itskin discloses an interconnect apparatus comprising a plurality of upper level cache controllers, and where each upper level cache controller is capable of controlling operation of the allocable cache memory blocks as a writeback cache [L2 *controllers connected to system bus*; Fig. 2; *L2 controller monitors system bus as is well known in a write back design*; col. 3, lines 50-67].

It would have been obvious to one of ordinary skill in the art, having the teachings of Otterness and Akashi and Liao and Dean and Itskin before him at the time the invention was made, to modify the system of Otterness and Akashi and Liao and Dean to include an interconnect apparatus comprising a plurality of upper level cache controllers, and where each upper level cache controller is capable of controlling operation of the allocable cache memory blocks as a writeback cache because it would have maintained cache coherency in the system by monitoring the system bus during

memory reads by other processors because of the possibility that the cache may contain the only copy of data for the location, referred to as modified data [col. 3, lines 64-67] as taught by Itskin.

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Otterness et al (US6,460,122) and Akashi et al (US6,438,658) and Liao et al. (US6,681,296) and Dean et al (US6,604,174) and further in view of Applicant's Admitted Prior Art (hereinafter "AAPA").

As per claim 7, the combination of Otterness and Akashi and Liao and Dean discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Otterness and Akashi and Liao and Dean does not specifically teach a step of billing customers according to processor time and allocated cache as recited in the claim.

AAPA discloses a step of billing customers according to processor time and allocated cache [Background, page 3, section [0014]].

It would have been obvious to one of ordinary skill in the art, having the teachings of Otterness and Akashi and Liao and Dean and AAPA before him at the time the invention was made, to modify the system of Otterness and Akashi and Liao and Dean to include a step of billing customers according to processor time and allocated cache because it would have provided better machines to customers in that each partition may be dedicated to particular users and applications, and problems (such as crashes) that

arise in one partition need not adversely affect operation in other partitions as taught by AAPA.

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Otterness et al (US6,460,122) and Akashi et al (US6,438,658) and Liao et al. (US6,681,296) and Dean et al (US6,604,174) and further in view of Noel et al (US6,381,682).

As per claim 11, the combination of Otterness and Akashi and Liao and Dean discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Otterness and Akashi and Liao and Dean does not specifically teach the steps of stopping execution of operating systems in each partition, and restarting execution of operating systems in each partition, and wherein the system is capable of being repartitioned without rebooting each operating system as recited in the claim.

Noel discloses steps of stopping execution of operating systems in each partition [*CPUs assigned to each partition can be turned off dynamically*; col. 2, lines 60-65], and restarting execution of operating systems in each partition [*CPUs assigned to each partition can be turned on dynamically*; col. 2, lines 60-65], and wherein the system is capable of being repartitioned without rebooting each operating system [*the partitions can be changed without rebooting the system*; col. 4, lines 49-55].

It would have been obvious to one of ordinary skill in the art, having the teachings of Otterness and Akashi and Liao and Dean and Noel before him at the time the invention was made, to modify the system of Otterness and Akashi and Liao and Dean to include the steps of stopping execution of operating systems in each partition, and restarting execution of operating systems in each partition, and wherein the system is capable of being repartitioned without rebooting each operating system because it would have provided improved flexibility, resource availability and scalability by allowing multiple instances of operating system to execute cooperatively and by allowing the partitioning of resources to be performed by assigning resources within a configuration [col. 4, lines 25-40] as taught by Noel.

Response to Arguments

11. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach cache partitioning, parallel caches and cache allocating and fetching cache instructions and data from random access memory.

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 3/18/04

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Pierre M. Vital
Art Unit 2188
March 14, 2004